A New High Efficiency Current Source Driver With Bipolar Gate Voltage

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***Abstract*—A novel bipolar current source driver (CSD) for power MOSFETs is proposed in this paper. The proposed bipolar CSD alleviates the gate current diversion problem of the existing CSDs by clamping the gate voltage to a flexible negative value (such as –3.5 V) during turn-off transition. Therefore, the proposed driver is able to turn off the MOSFET much faster with a higher effective gate current. The idea presented in this paper can also be extended to other CSDs to further improve the efficiency with high output currents. The experimental results verify the benefits of the proposed CSD. For buck converters with 12 V input at 1 MHz switching frequency, the proposed driver improves the efficiency from 80.5% using the existing CSD to 82.5% (an improvement of 2%) at 1.2 V/30 A, and at 1.3 V/30 A output, from 82.5% using the existing CSD to 83.9% (an improvement of 1.4%).**

***Index Terms*—Buck converter, common source inductance, current diversion problem, current source driver (CSD), resonant gate driver (RGD), voltage regulators (VRs), voltage source driver (VSD).**

I. Introduction

THE next-generation voltage regulators (VRs) feature low output voltage, high output current, and high power density [1]–[3]. To meet the requirements of future microprocessors, it is necessary to increase the switching frequency to as high as possible (>1 MHz) within practical constraints, in order to reduce the size of passive components and achieve better dynamic performance [4]–[6].

However, as the switching frequency increases, the efficiency of a buck converter using the conventional voltage source driver (VSD) suffers from two main types of frequency-dependent losses: 1) gate drive loss, and 2) switching loss [7]–[9]. In addition, the impact of parasitic inductance, consisting of the printed circuit board (PCB) trace inductance and the bonding wire inside the MOSFET package, becomes even worse at higher frequency, which significantly introduces extra switching loss [10]–[13].

One way to reduce the gate drive loss is the use of resonant gate drivers (RGDs) [14]–[17], which can recover part of the gate drive energy. RGDs are especially effective for the synchronous rectifier (SR) of synchronous buck converters, since the SR is designed with large gate charge and small on-resistance, to reduce its conduction loss during freewheeling mode. Also, some RGDs can drive two MOSFETs with the transformer or coupled inductor [17], [18]. Unfortunately, the design of the transformer or the coupled inductor is really challenging. Most importantly, RGDs emphasize reduction of gate loss, but they can hardly reduce the switching loss that is the dominant loss for high-frequency operations. Therefore, the efficiency improvement potentials for RGDs are limited.

Current source drivers (CSD) that can reduce the switching loss of the power MOSFET are reported in [19]–[26] to improve the performance of RGDs. Either working under continuous current mode [19]–[22] or discontinuous current mode [23]–[26], the existing CSDs can charge and discharge the power MOSFET with a nearly constant current to accelerate the switching speed. In particular, during the turn-off transition where the majority of the switching loss occurs [11], [19], [27], the existing CSDs can turn off the power MOSFET with a negative voltage (around –0.7V). In other words, compared with the conventional VSDs whose gate drive signal is unipolar, the existing CSDs can achieve a bipolar gate driver signal, which means much faster switching speed and smaller switching loss. In order to further improve the performance of the CSD in the previous papers, a new bipolar CSD that can turn off the power MOSFET with a flexible negative voltage (such as –3.5 V) is proposed in this paper.

The outline of this paper is as follows. In Section II, the limitation of the existing gate drivers (conventional VSD and existing CSDs) during the turn-off transition is illustrated. Specifically, the current diversion problem of the existing CSDs introduced by the common source inductance is analyzed. Section III reports the topology and the operation principle of the proposed bipolar CSD, and summarizes its advantages. In Section IV, the experimental results are presented to verify the features of the proposed CSD, followed by discussions. Finally, the conclusion is drawn in Section V.

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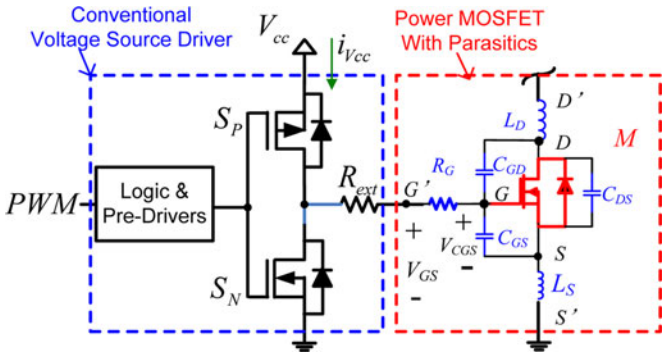


Fig. 1. Conventional VSD with the power MOSFET and its associated parasitics.

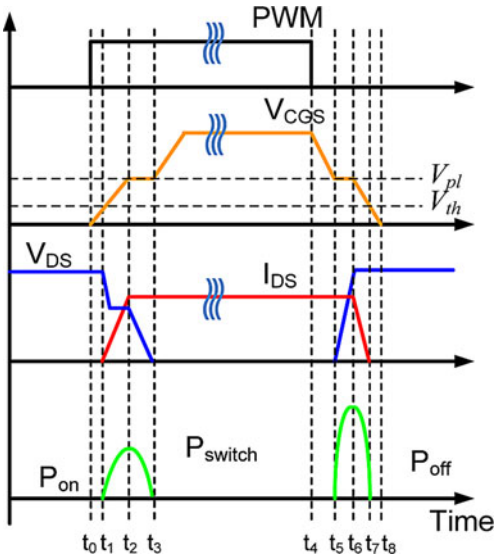


Fig. 2. Switching waveforms of the power MOSFET driven by the conventional VSD.

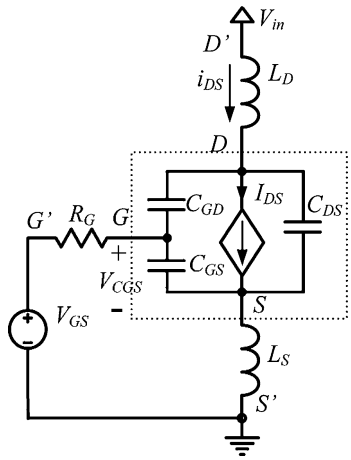


Fig. 3. Equivalent circuit of the MOSFET driven by the VSD during the turn-off transition.

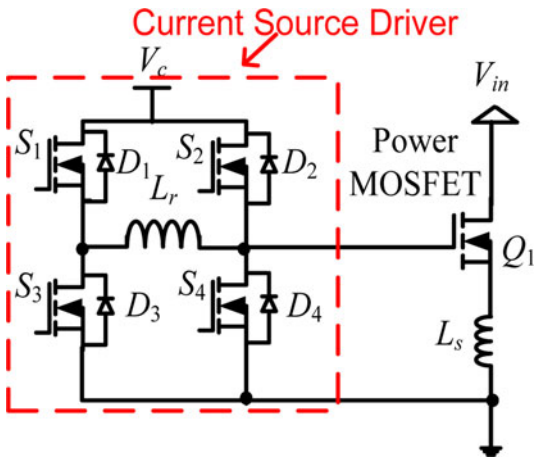


Fig. 4. Topology of the CSD reported in [23] and [24].

II. Limitation of the Existing Gate Drivers

A. Limitation of Conventional VSDs

The conventional VSD is illustrated in Fig. 1 to drive the power MOSFET, M, whose parasitics are shown: R_G is the gate resistance, $C_{\rm GS}$ is the gate-to-source capacitance, $C_{\rm GD}$ is the gate-to-drain capacitance, $C_{\rm DS}$ is the drain-to-source capacitance, and L_S is the common source inductance including the bonding wire inside the MOSFET package and PCB trace inductance, and L_D is the switching loop inductance. The conventional VSD has a totem pole configuration, which turns on the MOSFET by turning on the top switch of the VSD, S_P, while it turns off the MOSFET by turning on the bottom switch of the VSD, S_N.

The switching waveforms associated with Fig. 1 are shown in Fig. 2, where PWM is the PWM signal input of the VSD, $V_{\rm CGS}$ is the voltage across the $C_{\rm GS}$ of M, $V_{\rm DS}$ is the drain-to-source voltage across M, $i_{\rm DS}$ is the drain-to-source current flowing through the M, $P_{\rm on}$ is the turn-on loss, and $P_{\rm off}$ is the turn-off loss. It is noted that turn-off loss is the dominant loss of the total switching loss $P_{\rm switch}$ [11], [19], [27]. It is also observed that, due to the effect of the parasitic inductance, $V_{\rm DS}$ reduces sharply when $i_{\rm DS}$ starts to increases at t_1 and then keeps almost constant during (t_1, t_2) since the rising rate of $i_{\rm DS}$ is almost constant in this interval [11], [12].

The equivalent circuit of the MOSFET driven by the VSD during the turn-off transition is given in Fig. 3. When S_N in Fig. 1 is turned ON, because of the on-resistance of S_N (larger than 0.5 Ω), the voltage appearing across the gate-to-source of the power MOSFET, $V_{\rm GS}$, is around 0.5 V. Therefore, the main drawback of the VSD is that $V_{\rm GS}$ is unipolar, which means that $V_{\rm GS}$ is always bigger than zero, even during the turn-off transition. This seriously limits the turn-off speed, especially in the presence of the common source inductance in high-frequency application as described in the following section.

B. Limitation of the Existing CSDs (Current Diversion Problem)

The CSD circuits, either working under continuous current mode or discontinuous current mode, can turn on and turn off the power MOSFET with a nearly constant current. One of the representative CSDs is reported in [23] and [24]. As shown in Fig. 4, it has the following advantages.

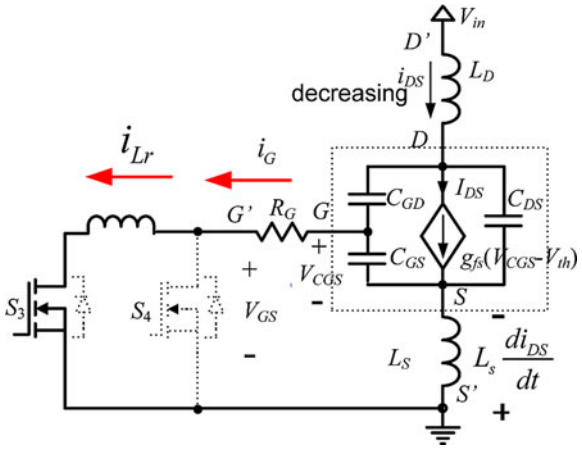


Fig. 5. Simplified discharging circuit of the existing CSD in [23] and [24].

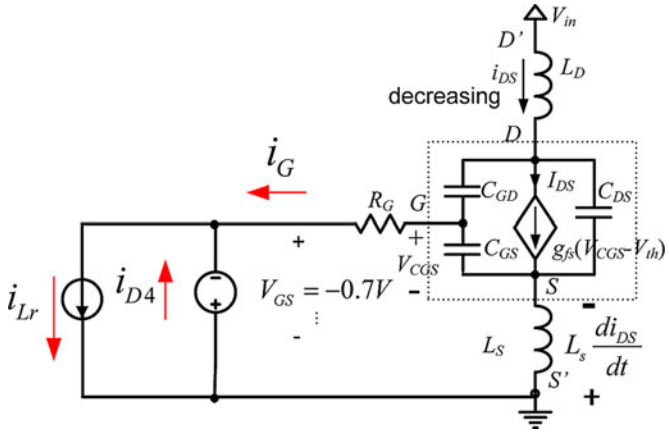


Fig. 6. Equivalent circuit of the CSD in [23] and [24] after *D*4 is ON.

1) Minimized circulating current and thus minimal conduction loss.
2) Independent of the duty cycle, suitable for narrow duty cycle operation.
3) Lower inductor value, easier for integrated circuit (easier for integration).
4) Soft switching of the driver switches.

However, the CSDs previously proposed have the same gate current diversion problem during the switching transition due to the impact of the common source inductance. Since the turn-off loss dominates the switching loss, the turn-off transition is the focus of this paper. During the turn-off transition, the CSD in Fig. 4 can be simplified as the circuit in Fig. 5. The gate-to-source voltage $V_{\rm GS}$ in Fig. 5 is derived as follows:

$$V_{\rm GS} = -i_{\rm G} R_G + V_{\rm CGS} - L_s \frac{di_{\rm DS}}{dt} \tag{1}$$

where $V_{\rm CGS}$ represents the voltage across the gate-to-source capacitance of the MOSFET Q, i_G is the effective discharge current, and $i_{\rm DS}$ represents the drain-to-source current.

The higher the drain current falling rate $di_{\rm DS}/dt$, the faster the turn-off transition is achieved. According to the relationship in (1), $V_{\rm GS}$ decreases when $di_{\rm DS}/dt$ increases. However, when $V_{\rm GS}$ goes below –0.7 V, the body diode of S_4, D_4, in Fig. 4 will conduct, clamping $V_{\rm GS}$ at –0.7 V. The equivalent circuit of the CSD after D_4 is driven on as shown in Fig. 6. It is noted that, compared with the VSD whose gate-to-source voltage is unipolar, the $V_{\rm GS}$ of the existing CSDs is bipolar waveform, which means that the CSD can achieve faster turn-off speed than the VSD because of the negative $V_{\rm GS}$ (–0.7 V).

After D_4 is on, part of the inductor current $i_{\rm Lr}$ is diverted through D_4, and the current diversion problem, which commonly exists in the existing CSDs, occurs. Thus the falling rate of the drain current, $di_{\rm DS}/dt$, is limited. Therefore, the effective discharge current i_G derived in (2) is reduced, which increases the turn-off transition time and weakens the effectiveness of the CSD

$$i_G = i_{\rm Lr} - i_{D4} \tag{2}$$

where i_G is the gate discharge current, i_{Lr} is the current flowing in the inductor, and i_{D4} is the current diverted through the body diode D_4. It should be noted that, due to the effect of L_s, the gate current diversion problem becomes even worse under a high load current condition.

To validate the analysis regarding the limitation of the CSD in [23] and [24], computer simulation is conducted with SIMetrix [28]. The waveforms of $V_{\rm CGS}, V_{\rm DS}, i_{\rm DS}, i_{\rm Lr}, i_G$ and the current diverted through the body diode D_4, i_{D4}, are shown in Fig. 7. There are three intervals of the turn-off transition shown in Fig. 7: 1) turn-off delay (t_0, t_1); 2) Miller plateau (t_1, t_2); and 3) drain current drop (t_2, t_3). It is observed that during turn-off delay and Miller plateau there is no current diversion problem as $i_{\rm DS}$ does not change during these two intervals, while when $i_{\rm DS}$ decreases during (t_2, t_3), a large portion of current out of 2.5 A peak current source inductor current is diverted through the body diode D_4 because of the impact of L_s, which significantly limits the turn-off speed.

III. Proposed Bipolar Current Source Driver Circuit

A. Proposed Bipolar Current Source Driver

In order to alleviate the gate current diversion problem mentioned above and reduce the switching loss, a new bipolar CSD that can turn off the MOSFET with a flexible negative voltage is proposed in this paper. The topology of the proposed CSD is given in Fig. 8. It is noted that compared with the CSD in Fig. 4, S_4 is replaced by a pair of four-quadrant switches, S_4 and S_5, whose source terminals are connected together to block the conduction of body diodes. Another key feature of the proposed CSD is to use five diodes D_{s1}–D_{s5} as an antidiode of the S_4 and S_5 branch to create a negative gate voltage (i.e., –3.5 V in Fig. 8) during the turn-off transition, which can noticeably increase the gate discharge current. It is noted that the number of the diodes used in the proposed bipolar CSD is flexible and dependent on the value of the negative voltage designed during the turn-off transition.

The waveforms of the five switch gate driving signals, $V_{\rm GS1}$–$V_{\rm GS5}$, the inductor current $i_{\rm Lr}$, the gate charge/discharge current i_G, the voltage across $C_{\rm GS}$–$V_{\rm CGS}$, the drain-to-source

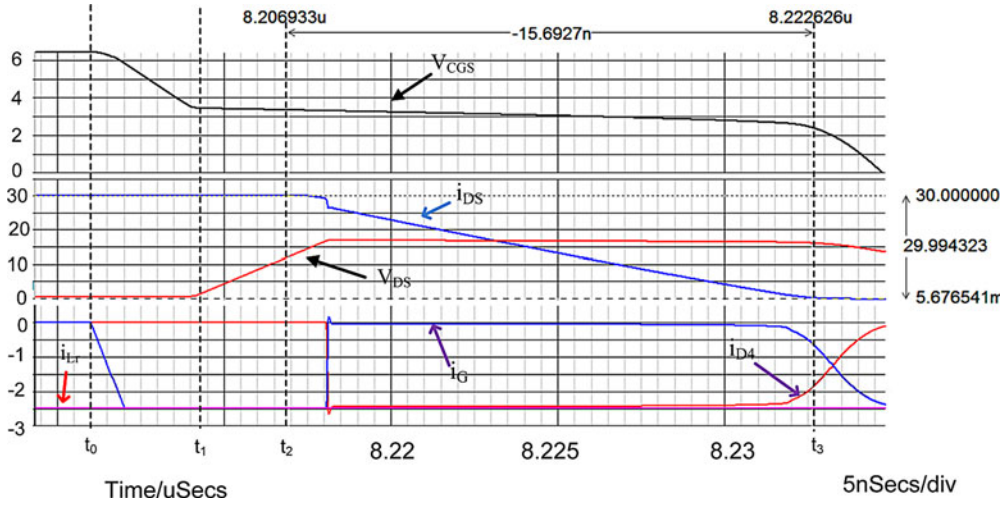


Fig. 7. Simulation waveforms of the turn-off transition of the CSD in [23] and [24].

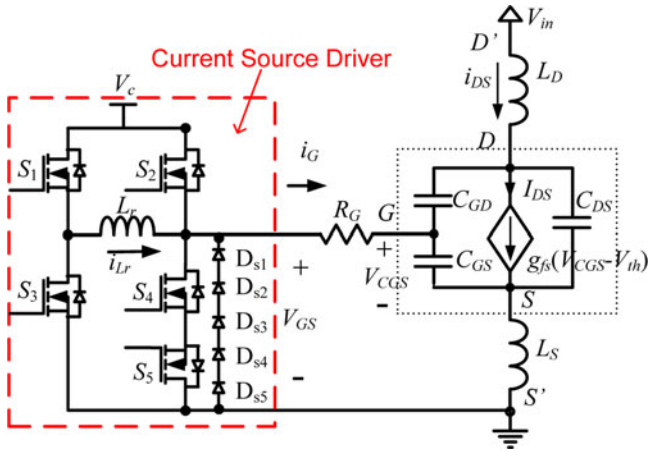


Fig. 8. Power MOSFET driven by the proposed bipolar CSD.

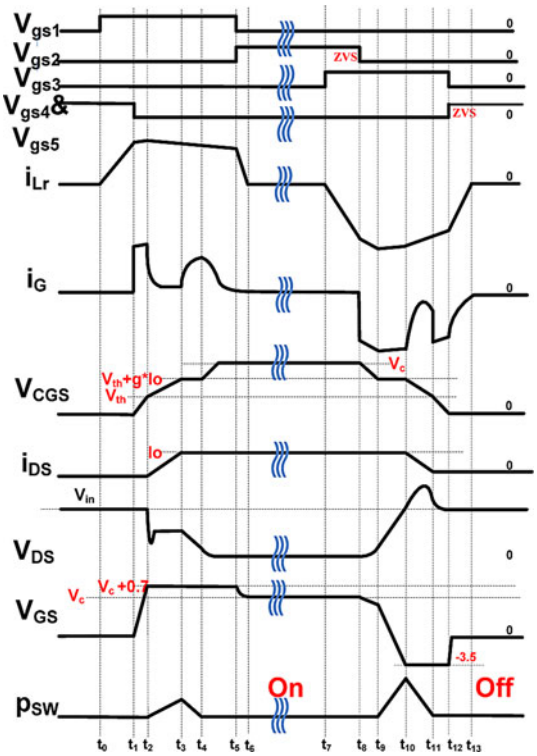


Fig. 9. Waveforms of the proposed bipolar CSD.

current $i_{\rm DS}$, the drain-to-source voltage $V_{\rm DS}$, and the gate-to-source voltage $V_{\rm GS}$ are illustrated in Fig. 9. It is noted the gate signals for S_4 and S_5 are exactly the same all through the switching cycles.

B. Detailed Turn-On Operation

The operation principle of the turn-on transition is illustrated as follows. Prior to t_0, the power MOSFET is assumed to be in the OFF state, and S_4 and S_5 are in the ON state.

1) *Turn-on precharge (t_0, t_1):* At t_0, S_1 is turned ON, and the inductor current $i_{\rm Lr}$ rises almost linearly in the positive direction through the current path shown in Fig. 10(a). The precharge state ends at t_1, which is usually set by the designer.
2) *Turn-on delay (t_1, t_2):* At t_1, S_4 and S_5 are turned OFF, the inductor current $i_{\rm Lr}$ starts to charge the gate capacitance of Q—the equivalent circuit is given in Fig. 10(b). At this interval, the effective charge current i_G equals $i_{\rm Lr}$. This interval ends when $V_{\rm CGS}$ reaches $V_{\rm th}$.
3) *Drain current rising (t_2, t_3):* At t_2, $V_{\rm CGS} = V_{\rm th}$. During this interval, $V_{\rm CGS}$ keeps increasing, and $i_{\rm DS}$ starts to rise according to the relationship in (3). Since $i_{\rm DS}$ flows through L_S, according to (1), the large voltage induced across L_S makes $V_{\rm GS}$ far larger than the driver supply voltage V_c. Therefore, D_2, the body diode of the driver switch S_2, is driven on to clamp $V_{\rm GS}$ at V_c +0.7. The equivalent circuit is shown in Fig. 10(c). At this interval, i_G drops sharply because of the voltage clamping. The subtraction of $i_{\rm Lr}$ and i_G is diverted through D_2

$$i_{\rm DS} = g_{\rm fs}(V_{\rm CGS} - V_{\rm th}) \tag{3}$$

where $g_{\rm fs}$ is the transconductance of the power MOSFET.

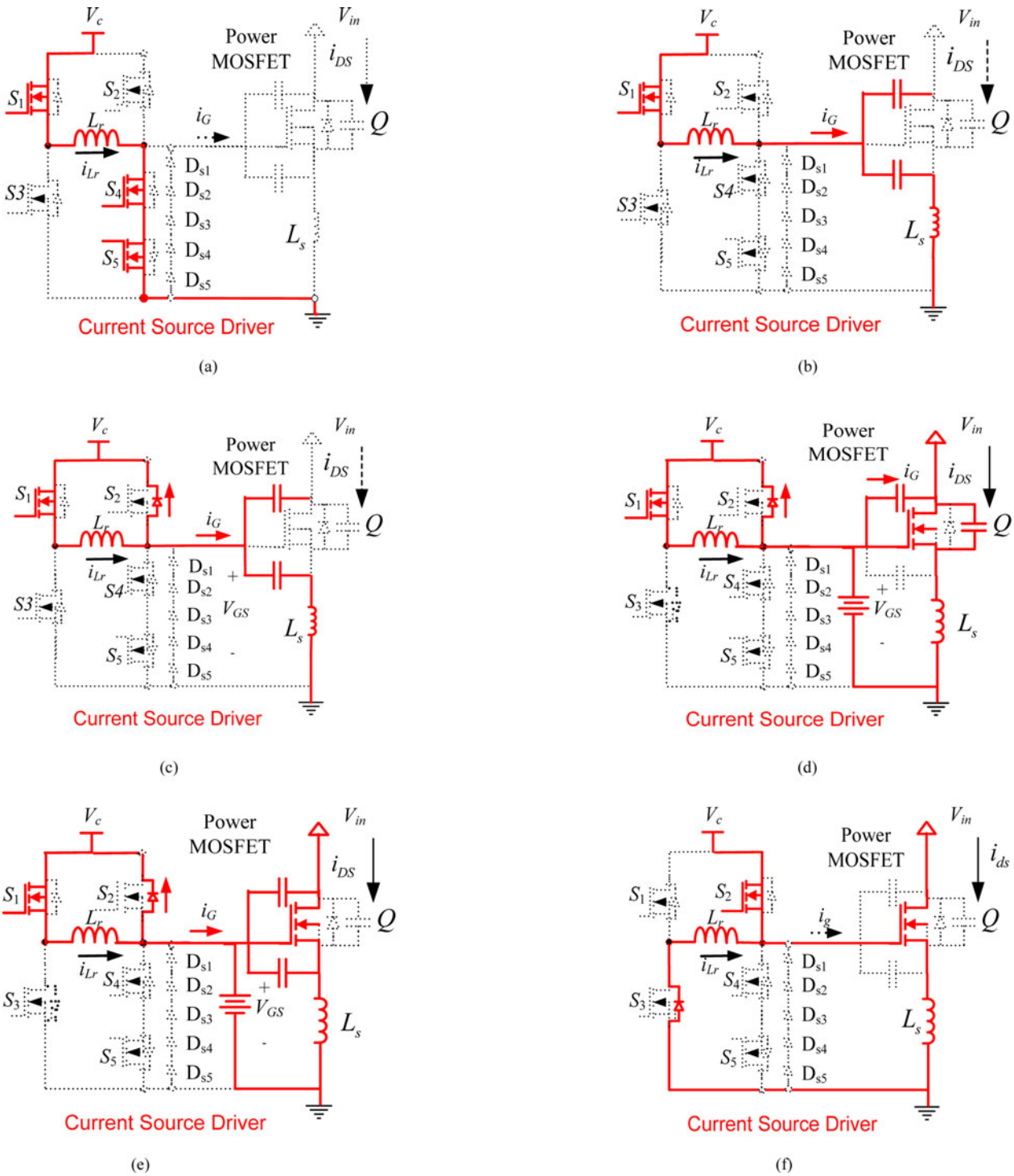


Fig. 10. Turn-on operation. (a) (t_0, t_1): Precharge. (b) (t_1, t_2): Turn-on delay. (c) (t_2, t_3): Drain current rising. (d) (t_3, t_4): Miller plateau. (e) (t_4, t_5): Remaining Gate Charging. (f) (t_5, t_6): Energy recovery.

4) *Miller plateau (t_3, t_4):* At t_3, $i_{\rm DS} = I_o$. During this interval, $V_{\rm CGS}$ is held at the Miller plateau voltage. i_G mainly flows through the gate-to-drain capacitance of Q, and $V_{\rm DS}$ decreases accordingly. It is noted that i_G starts to rapidly increase since the EMF across L_s falls sharply due to the unchanged $i_{\rm DS}$; however, part of the inductor current is still diverted through D_2. The equivalent circuit is given in Fig. 10(d).
5) *Remaining gate charging (t_4, t_5):* At t_4, $V_{\rm DS} = 0$ and $V_{\rm CGS}$ starts to rise again until it reaches V_c. $V_{\rm GS}$ remains at V_c $+0.7$, and due to the rising of the $V_{\rm CGS}$, i_G decreases gradually. The equivalent circuit is given in Fig. 10(f).
6) *Energy recovery (t_5, t_6):* At t_5, S_2 is turned ON to recover the energy stored in the inductor to the source as well as actively clamping Q to V_c. It is noted that the gate voltage of the power MOSFET is clamped to V_c through a low

impedance path, which prevents the circuit being false triggered by the *Cdv*/*dt* effect.

C. Detailed Turn-Off Operation

The operation principle of the turn-off transition is illustrated as follows. Prior to t_7, the power MOSFET is assumed to be in the ON state and S_2 is also in the ON state.

1) *Turn-off precharge (t_7, t_8):* At t_7, S_3 is turned ON, and the inductor current $i_{\rm Lr}$ rises almost linearly in the negative direction through the current path shown in Fig. 11(a). The precharge state ends at t_8, which is set by the designer, and S_2 is turned OFF with zero voltage switching (ZVS) at t_8.
2) *Turn-off delay (t_8, t_9):* At t_8, S_2 is turned OFF. In this interval, $V_{\rm CGS}$ decreases until $V_{\rm th} + I_o * g_{\rm fs}$, which ends the interval. The equivalent circuit is given in Fig. 11(b).
3) *Miller plateau (t_9, t_{10}):* At t_9, $V_{\rm CGS} = V_{\rm th} + I_o * g_{\rm fs}$. In this interval, $V_{\rm CGS}$ holds at the Miller plateau voltage, $V_{\rm th} + I_o * g_{\rm fs}.i_G$ (equal to $i_{\rm Lr}$) strictly discharges the gate-to-drain capacitance $C_{\rm GD}$ of Q, and $V_{\rm DS}$ rises until it reaches $V_{\rm in}$ at t_{10}. The equivalent circuit is illustrated in Fig. 11(c).
4) *Drain current drop (t_{10}, t_{11}):* At t_{10}, $V_{\rm DS} = V_{\rm in}$ and $V_{\rm CGS}$ continues to decrease from $V_{\rm th} + I_o * g_{\rm fs}$ to $V_{\rm th}$.$i_{\rm DS}$ falls from I_o to zero according to the relationship in (3). According to (1), due to the induction EMF across L_s, the series connected diodes D_{s1}–D_{s5} are driven on to clamp $V_{\rm GS}$ at around –3.5 V. The voltage across the current source inductor becomes –3.5 V, so $i_{\rm Lr}$ decreases at a higher rate than in the turn-on transition. The equivalent circuit of this interval is given in Fig. 11(d). It is emphasized is that the CSD proposed in [23] and [24] only can clamp $V_{\rm GS}$ to –0.7 V. This means that the turn-off speed of the CSD proposed in this paper is much faster than that of the CSD in [23] and [24]. It is worth mentioning that $V_{\rm DS}$ in this interval will keep rising due to the effect of L_s.
5) *Remaining gate discharging (t_{11}, t_{12}):* At t_{10}, $V_{\rm CGS} = V_{\rm th}$. In this interval, $V_{\rm CGS}$ continues to decrease until it equals zero. It is noted that $V_{\rm DS}$ continues to rise during this interval. The equivalent circuit is shown in Fig. 11(e).
6) *Energy recovery* (t_{12}, t_{13}): At t_{12}, S_3 is turned OFF and S_4 and S_5 are turned ON with ZVS. The body diode of S_1, D_3, is forced on by $i_{\rm Lr}$, and the CSD circuit turns into the mode of energy recovery through the path shown in Fig. 11(f). During this interval, the energy stored in L_r is recovered to V_c. The interval ends at t_{13} when the inductor current becomes zero.

The detailed switching transition is analyzed above. The current diversion problem introduced by the common source inductance is addressed. It is noted that the current diversion problem exists in both turn-on and turn-off transitions. However, since the turn-off loss is the dominant loss of the switching loss, only the current diversion in the turn-off transition is addressed. It could be concluded that the proposed CSD can achieve bipolar gate drive waveforms because of the diversion of the D_{s1}–D_{s5} during the turn-off transition.

D. Advantages of the Proposed Bipolar CSD

The proposed CSD circuit in this paper has the following advantages.

1) Significantly Reduced Turn-Off Time and Thus Turn-Off Loss: During the turn-off transition, the gate discharge current is not diverted through the diode set D_{s1}–D_{s5} until the gate voltage reaches a much lower voltage (–3.5 V) due to the increases or decreases of the current through the power MOSFET. When current decreases during the turn-off transition, $V_{\rm GS} = 0.5\,{\rm V}$ for the VSD because of the on-resistance of the driver switch, S_N, in Fig. 1; for the CSD in Fig. 4, $V_{\rm GS} = –0.7\,{\rm V}$ because of the conduction of D_4, while for the bipolar CSD in Fig. 8, $V_{\rm GS} = –3.5\,{\rm V}$ because of the conduction of D_{s1}–D_{s5}.

Simulations under the same condition for the VSD, the existing CSD in [23] and [24], and the proposed CSD, are conducted with SIMetrix to verify the benefit of the proposed CSD. In comparison with the turn-off waveforms of the existing CSD in Fig. 7, the turn-off waveforms of the proposed CSD are shown in Fig. 12. Fig. 13 summarizes the comparison of the current fall time and the average discharging current among the proposed CSD, existing CSD, and VSD. It is observed that, for the proposed CSD, it takes 8.7 ns for $i_{\rm DS}$ to decrease from 30 A to 0, which is about half the time needed for the existing CSD (15.6 ns) and one third the time needed for VSD (20.1 ns).

The reason for the significant improvement of the proposed CSD over the existing gate drivers (VSD and existing CSDs) is that the gate discharge current i_G of the proposed CSD is greatly increased. It is observed from Fig. 13 that the average discharge current i_G of the proposed CSD is four times that of the VSD and twice that of the existing CSD.

In order to support the simulation results above, calculations have been done with the piecewise linear approximation model [27]. According to the datasheet of power MOSEFT Si7386DP used in the simulation [29], gate resistance $R_G = 1.7\ \Omega$. The voltages across the L_s for the VSD, existing CSD, and proposed CSD during $i_{\rm DS}$ falling time are calculated and compared in Table I. i_G is obtained from Fig. 13; $V_{\rm CGS}$ is derived by (4) according to the piecewise linear approximation; $L_s di_{\rm DS}/dt$ is calculated through (1).

From Table I, it is observed that the $L_s di_{\rm DS}/dt$ of the proposed CSD is around twice that of the existing CSD in [23] and [24] and three times that of the conventional VSD. In other words, the proposed CSD can decrease the current $i_{\rm DS}$ at a speed twice that of the existing CSD and three times that of the VSD, which matches with the simulation results in Fig. 13

$$V_{\rm CGS} = \frac{V_{\rm pl} + V_{\rm th}}{2} \tag{4}$$

where $V_{\rm CGS}$ is the voltage across the gate-to-source capacitance of the MOSFET Q, $V_{\rm pl}$ means the Miller plateau voltage of Q, and $V_{\rm th}$ is the gate threshold voltage of Q.

2) Better Immunity to Voltage Across R_G: Compared with the VSD and the existing CSD in [23] and [24], the proposed CSD has better immunity to the voltage drop across R_G. As illustrated in Table I, the proposed CSD can handle 1.17 V voltage drop across R_G, while the VSD can only handle 0.27 V and the existing CSD can handle 0.43 V. The larger the voltage

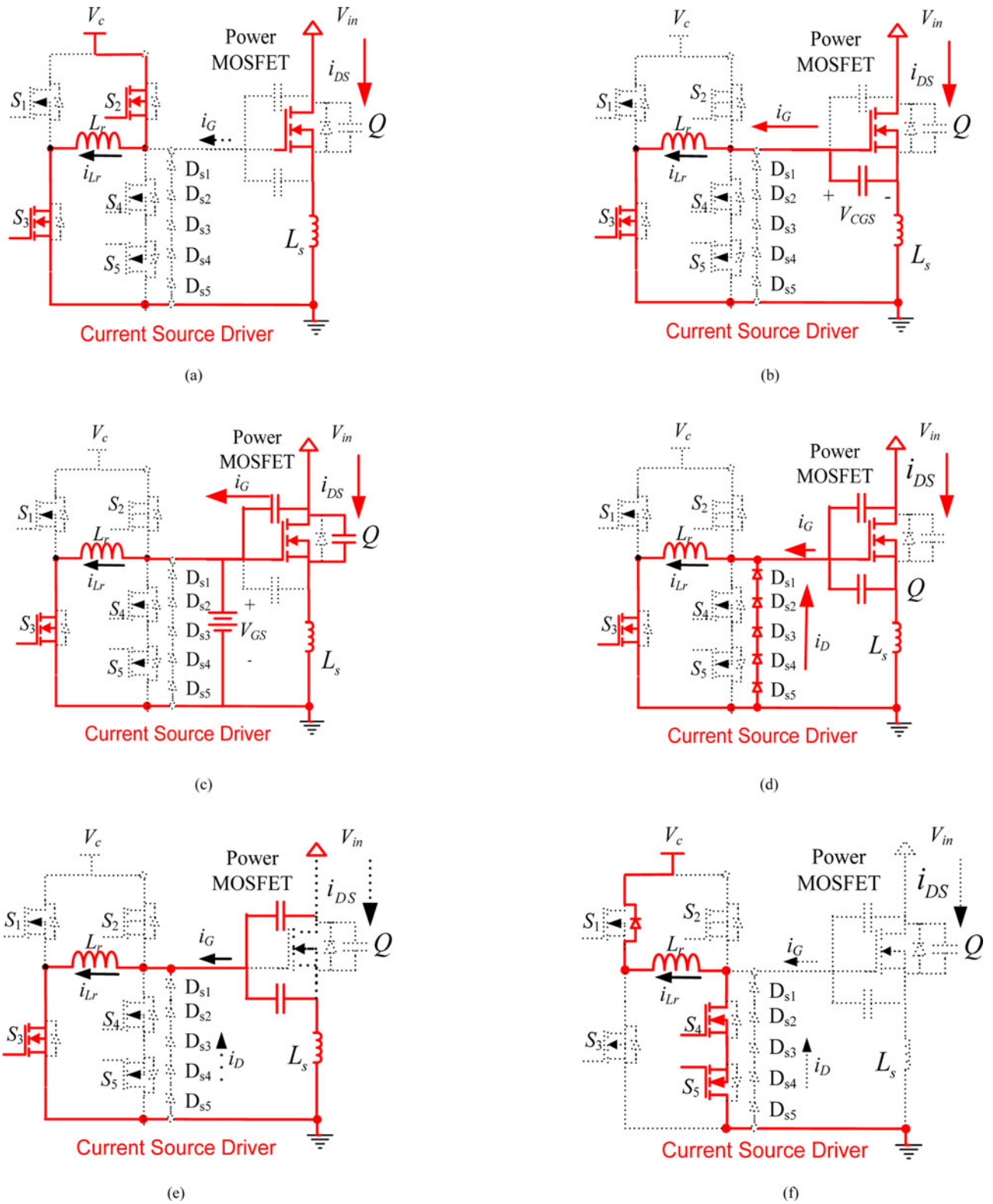


Fig. 11. Turn-off operation. (a) (t_7, t_8): Predischarge. (b) (t_8, t_9): Turn-off delay. (c) (t_9, t_{10}): Miller plateau. (d) (t_{10}, t_{11}): Drain current drop. (e) (t_{11}, t_{12}): Remaining gate discharge. (f) (t_{12}, t_{13}): Energy recovery.

drop the gate driver can handle, the faster turn-off speed it can achieve. Therefore, the proposed CSD can turn off the power MOSFET with a faster speed than VSD and the existing CSD in [23] and [24].

3) Less Impact of Parasitic Inductance: Whether in the conventional VSD or the existing CSDs, the parasitic inductance, especially common source inductance, significantly reduces the switching speed and hereby increases the switching loss [22].

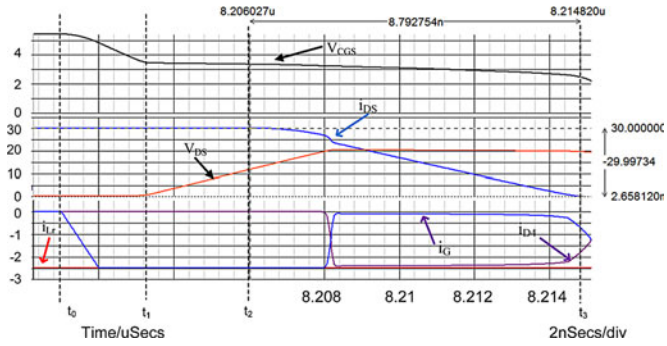


Fig. 12. Simulation waveforms of the turn-off transition of the proposed CSD.

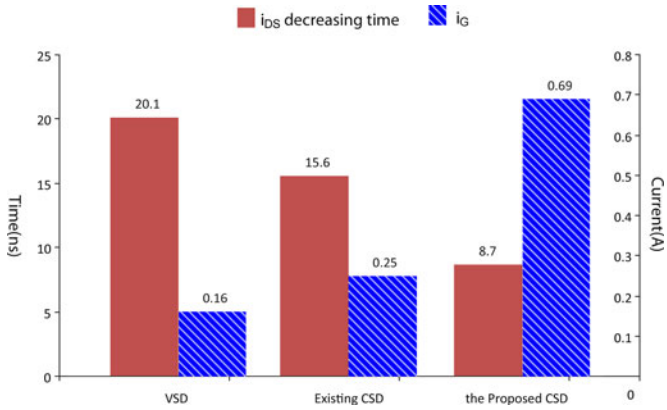


Fig. 13. Comparison of the simulated current fall time and the average discharging current

TABLE I
COMPARISON OF VSD, EXISTING CSD, AND PROPOSED CSD DURING TURN-OFF

Driver Type	V_{GS}	i_G	$i_G R_G$	V_{CGS}	$L_s di_{DS}/dt$
VSD	0.5 V	0.16 A	0.27V	2.7 V	1.93 V
Existing CSD	-0.7 V	0.25 A	0.43V	2.7 V	2.98 V
Proposed CSD	-3.5 V	0.69A	1.17V	2.7 V	5.03 V

The proposed bipolar CSD can well alleviate the impact of parasitic inductor with $V_{\rm GS}$ clamped to a flexible negative voltage (such as –3.5 V), which can reduce the turn-off time and hereby improve the efficiency.

4) Smaller Current Source Inductor: The CSD proposed in this paper works in discontinuous current mode, which allows the current source inductor to be very small (tens of nH). It is expected that, with better on-chip inductor techniques on the way, the CSD inductor can be fully integrated into the driver chip in the near future [30].

5) High Stability and Noise Immunity: The MOSFET is either actively clamped to V_c during on or to zero during off, which will minimize the possibility of the MOSFET being falsely triggered by the C*dv*/*dt* effect and increase the stability of the circuit.

6) Application Extension to Other CSDs: The idea presented in this paper can be used to further alleviate the gate current diversion problem during the turn-on transition. Fig. 14 shows the topology of a new bipolar CSD with an improved turn-on gate current. The CSD in Fig. 14 increases the gate current during the turn-on transition based on the same idea presented in this paper. However, it is noted that, since turn-on loss is relatively small compared with turn-off loss, the improvement of the CSD during the turn-on transition in Fig. 14 would be less significant than the improvement of the CSD during the turn-off transition proposed in this paper.

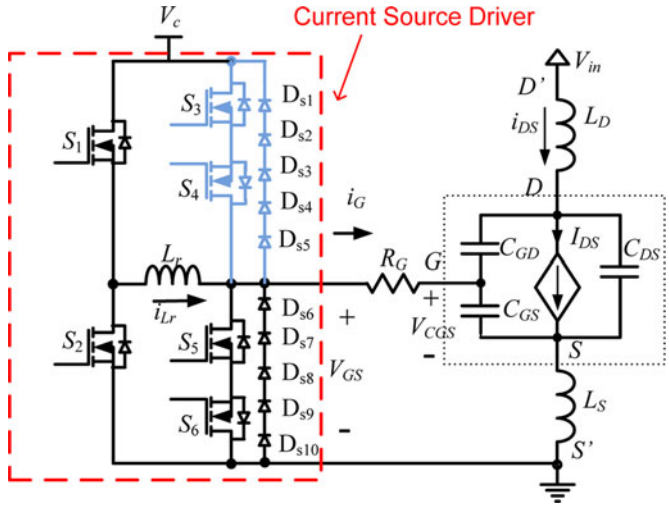


Fig. 14. New bipolar CSD with improved turn-on gate current.

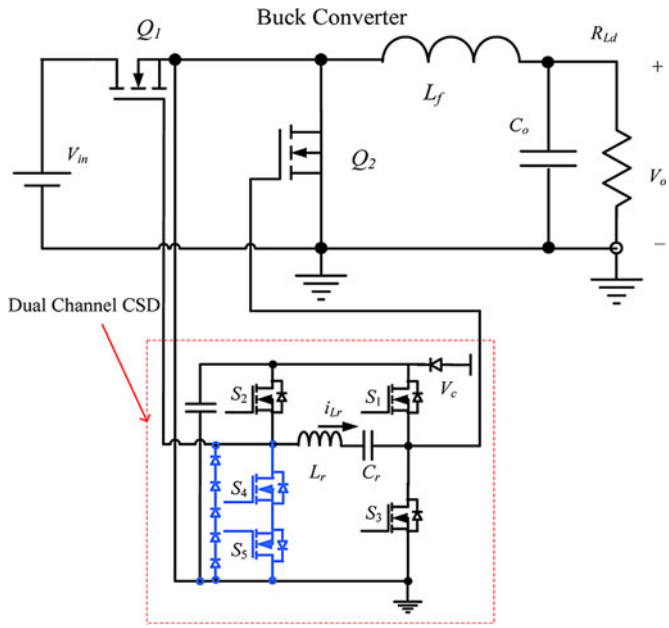


Fig. 15. Improved dual channel bipolar CSD with continuous inductor current mode.

Another advantage of the bipolar CSD proposed here is that it can be widely extended to all other existing CSDs to further improve the turn-off speed. Fig. 15 illustrates the improved bipolar CSD operating with continuous inductor current mode to drive both the control FET and SR of the synchronous buck converter [21], while another improved bipolar CSD with continuous inductor current mode is presented in Fig. 16, which enables the magnetic integration of inductors L_{r1} and L_{r2} [22].

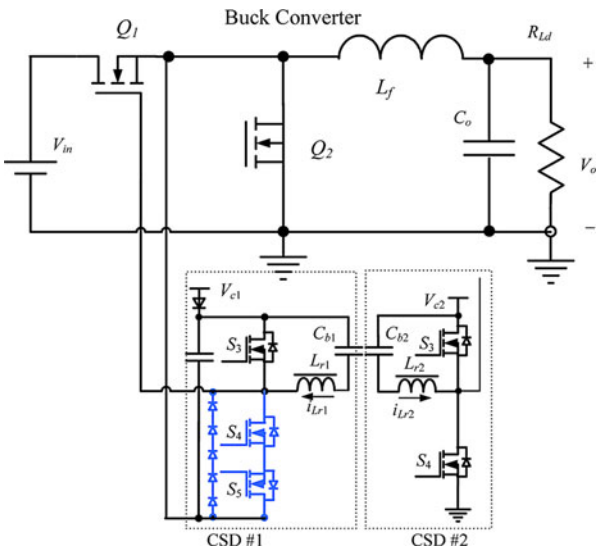


Fig. 16. Improved bipolar CSD working with continuous inductor current mode.

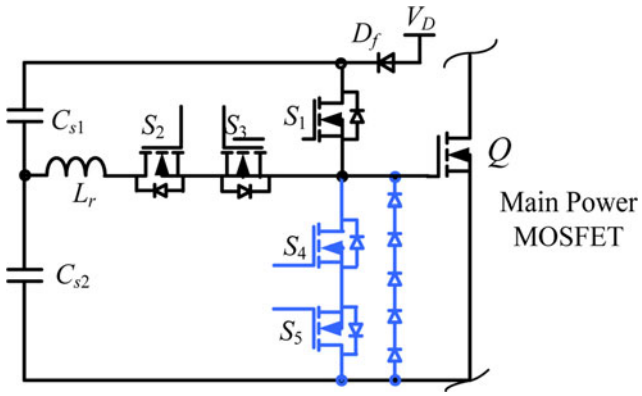


Fig. 17. Improved bipolar CSD working with discontinuous inductor current mode

In Fig. 17, a discontinuous inductor current mode CSD [26] is improved using the idea presented in this paper to achieve bipolar switching waveforms. It is noted that all the improved portions of the three CSDs are marked in blue.

IV. Experimental Verification and Discussion

A prototype for a synchronous buck converter shown in Fig. 18 was built to verify the advantages of the proposed CSD circuit. The control FET of the buck converter is driven by the proposed CSD, while the SR is driven by the conventional VSD as the switching loss of the SR is very small. The design parameters are given in Table II.

The photo of the prototype is shown in Fig. 19. It uses 6-layer, 4-oz copper PCB. Fig. 20 illustrates the hardware implementation of the proposed CSD. Altera Max II EPM240 Complex Programmable Logic Device (CPLD) is used to generate the pulse width modulation (PWM) signals with accurate delays since the CPLD can achieve time resolution as high as 1/3 ns per gate. Driver switches S_1–S_5 are driven with the level shift circuits.

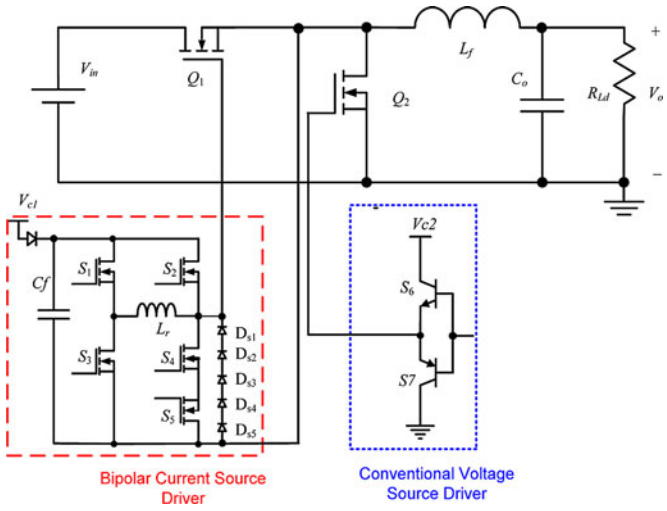


Fig. 18. Buck converter with the proposed bipolar CSD.

TABLE II
Design Parameters

Switching Frequency, f_s	1MHz
Input Voltage, V_{in}	12V
Output Voltage, V_o	1.2 and 1.3V
SR Gate Drive Voltage, V_{c2}	6.5V
SR, Q_2	IRF6691
CSD Voltage,V_{c1}	5V
Control FET, Q_1	Si7386DP
Output Inductor, L_f	330nH,Vishay IHLP5050CE
Driver Switches, $S_1 - S_5$	FDN335N
Driver Inductor, L_r	43nH,Coilcraft B10T_L
Diodes, $D_{s1} - D_{s5}$	MBR0520

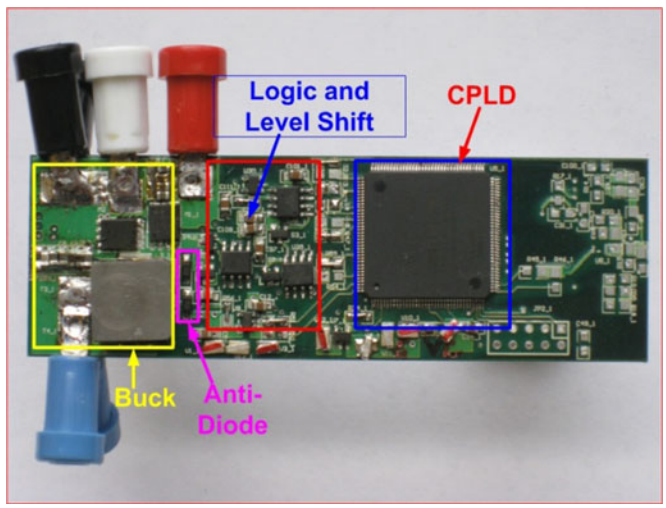


Fig. 19. Photo of prototype with the proposed bipolar CSD.

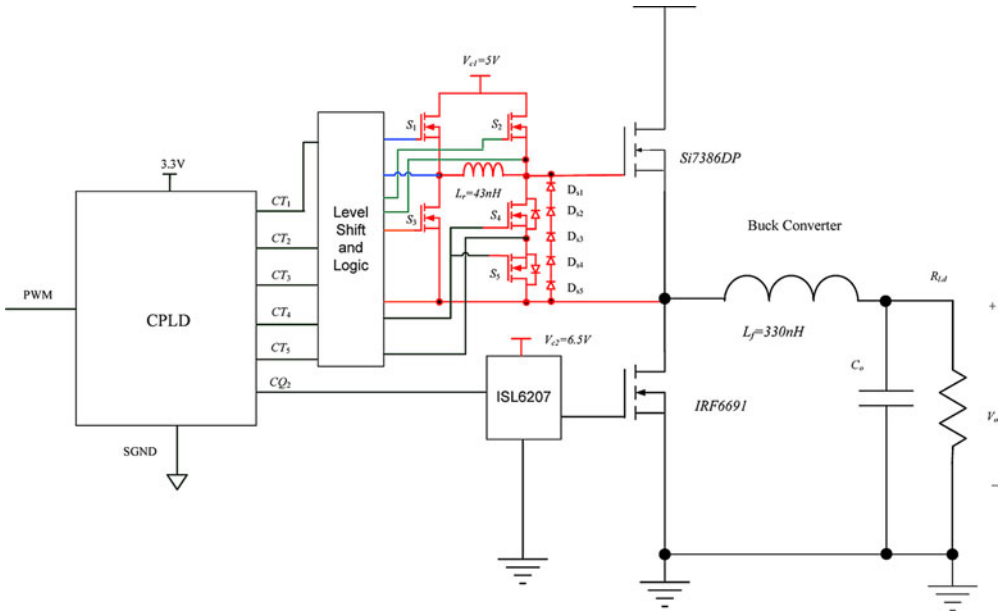


Fig. 20. Hardware implementation of the buck converter driven with the proposed CSD.

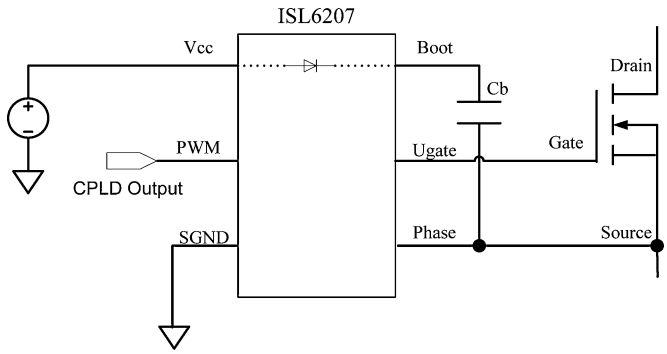


Fig. 21. Implementation of level shift circuits by ISL6207.

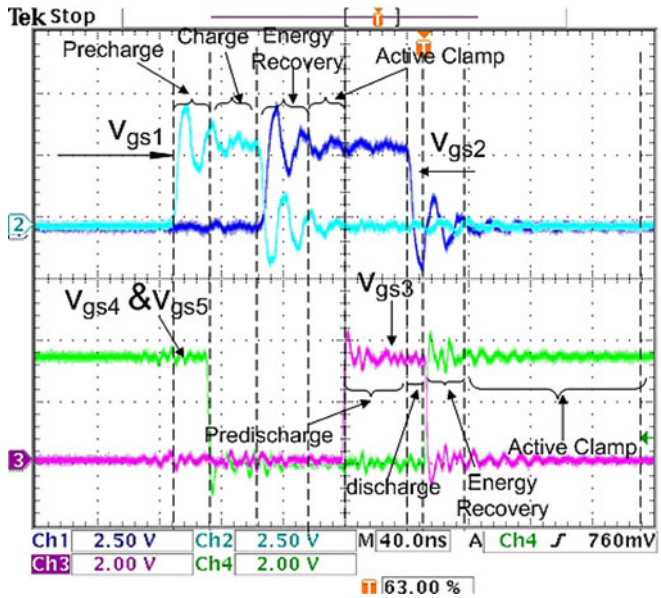


Fig. 22. Driver switch gate signals ($V_{\rm GS1}$–$V_{\rm GS5}$).

The level shift circuits for S_1–S_5 are implemented by discrete components from Intersil ISL6207 as shown in Fig. 21. The operating principle is as follows.

The voltage to turn on the driver switch (S_1–S_5) is supported by the capacitance C_b. The voltage across C_b is built up when the source terminal of the driver switch equals ground (GND), which allows C_b to be charged to V_c.

When the output of the CPLD is "high," the gate-to-source voltage of the driver switch equals the voltage across C_b, while when the PWM is "low," the gate-to-source voltage of the driver switch equals zero.

Fig. 22 shows switch gate signals, $V_{\rm GS1}$–$V_{\rm GS5}$ and associated modes for turn-on and turn-off transition, respectively.

Fig. 23 illustrates the driver inductor current $i_{\rm Lr}$ and the gate-to-source voltage $V_{\rm GS\_Q1}$ of control FET. It can be observed that Q_1 is charged and discharged with nearly constant current and $V_{\rm GS\_Q1}$ is clamped to about –3.5 V during the turn-off transition. Most importantly, there is no Miller Plateau observed in $V_{\rm GS\_Q1}$. It is noted that the effective charge current, i_G, is difficult to measure without disturbing the circuit operation. Therefore, the measured waveform of i_G is not provided in this paper.

The gate to source voltage waveforms for control FET and SR are shown in Fig. 24. It is observed that the dead time between $V_{\rm GS\_Q1}$ and $V_{\rm GS\_Q2}$ is minimized to avoid body diode conduction without causing the shoot through problem.

Fig. 25 summarizes the measured efficiencies (including gate drive loss) of the proposed CSD in 1.2 V and 1.3 V output in 1 MHz switching frequency with 12 V input.

Fig. 26 shows the efficiency comparison among the proposed bipolar CSD, the existing CSD proposed in [23] and [24] and the conventional VSD at 12 V input, 1.2 V output, and 1 MHz switching frequency. It is noted that the proposed bipolar CSD

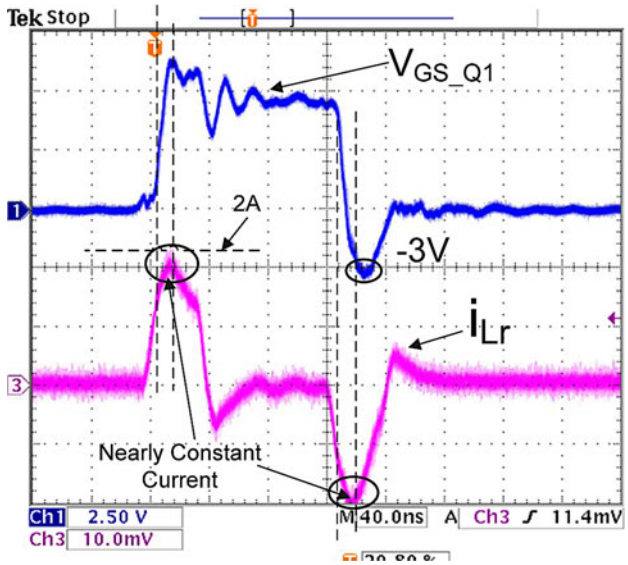


Fig. 23. V_{GS_Q1} and CSD inductor current I_{Lr}.

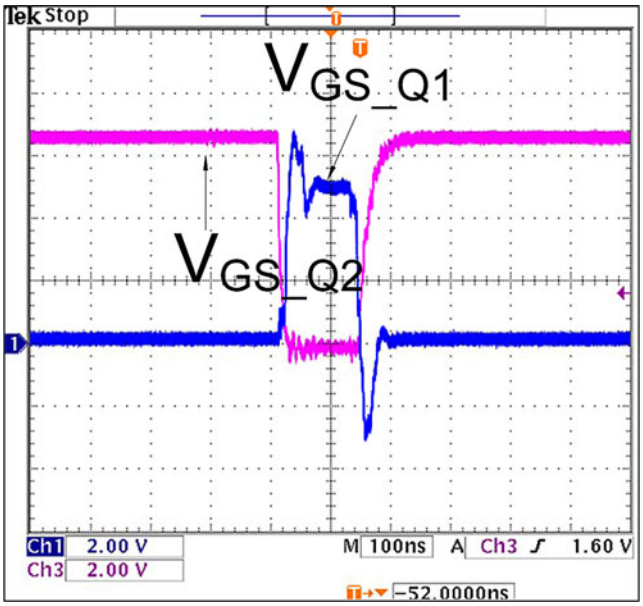


Fig. 24. V_{GS_Q1} and V_{GS_Q2}.

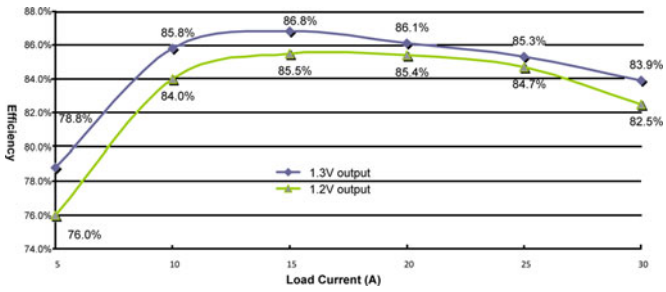


Fig. 25. Efficiencies at 12 V input, 1.2 V and 1.3 V output, and 1 MHz switching frequency.

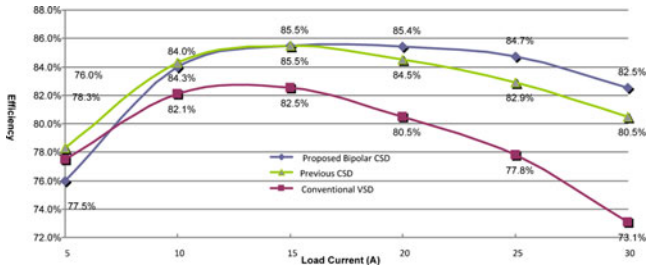


Fig. 26. Measured efficiency comparison at 12 V input, 1.2 V output, and 1 MHz switching frequency.

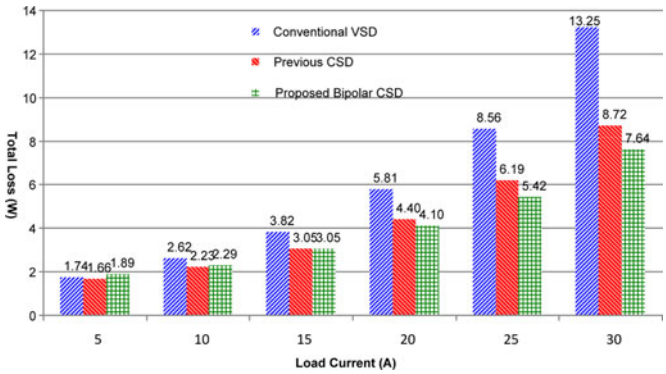


Fig. 27. Total measured loss comparison at 12 V input, 1.2 V output, and 1 MHz switching frequency.

increases the efficiency of the VSD from 73.1% to 82.5% by 9.4% at 1.2 V/30 A output and improves the efficiency of the existing CSD from 80.5% to 82.5% (by 2%) at 30 A output.

Fig. 27 compares the total measured loss (including gate drive loss) among the proposed bipolar CSD, the existing CSD proposed in [23] and [24], and the conventional VSD at 12 V input, 1.2 V output and 1 MHz switching frequency. It is noted that compared with the existing CSD, the proposed CSD saves a 1.08 W loss at 30 A load. While compared with the conventional VSD, the proposed CSD achieves a loss saving of 5.61 W at 30 A load.

Fig. 28 shows the efficiency comparison among the proposed bipolar CSD, the existing CSD proposed in [23] and [24], and the conventional VSD at 12 V input, 1.3 V output, and 1 MHz switching frequency. It is noted that, compared to the conventional VSD, the proposed bipolar CSD increases the efficiency of VSD from 77.5% to 83.9% (by 6.4%) and improves the efficiency of the existing CSD from 81.9% to 83.9% (by 2%) at 30 A output.

Fig. 29 compares the total measured loss (including gate drive loss) among the proposed bipolar CSD, the existing CSD proposed in [23] and [24], and the conventional VSD at 12 V input, 1.3 V output, and 1 MHz switching frequency. It is observed that the proposed bipolar CSD achieves a loss reduction of 3.84 W at 30 A load compared with the VSD. Even compared with the CSD in [23] and [24], the proposed bipolar CSD saves a loss of 1.14 W. It is also observed that the proposed CSD achieves higher efficiency improvement at high load current. This is because the proposed CSD significantly alleviates the gate current diversion problem at high current load.

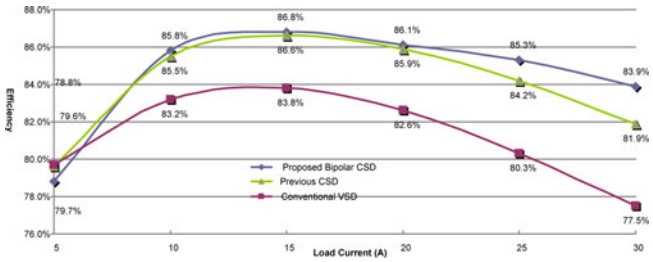


Fig. 28. Measured efficiency comparison at 12 V input, 1.3 V output, and 1 MHz switching frequency.

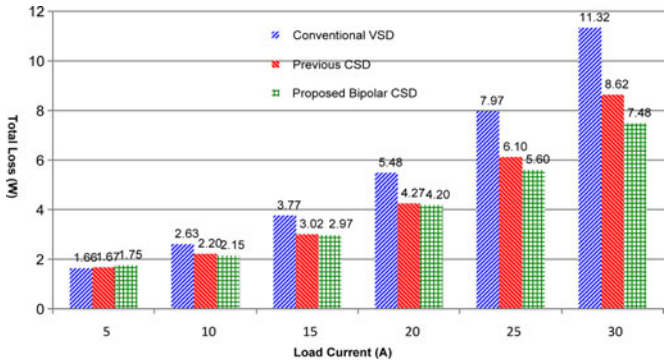


Fig. 29. Total measured loss comparison at 12 V input, 1.3 V output, and 1 MHz switching frequency.

The VR spends 20% of the time at the full load and the other 80% time at light load which is defined as any load below the full load [31]. The main aim of this paper is to propose a negative turn-off technology to reduce the switching loss. The proposed CSD has achieved visible improvement above 70% load, and it could also achieve high efficiency at other load by proper design. In light load, active phase number of the multiphase buck converter, can be reduced to make each phase operate at heavy load [32], [33] while in every light load (<10 A), the CSD can be disabled and replaced by the VSD to maintain high efficiency.

V. Conclusion

In this paper, a new bipolar CSD that can achieve much faster switching speed is proposed. The gate current diversion problem in the existing CSDs is analyzed. Compared with previous gate drivers (VSD and existing CSDs) the proposed CSD can turn off the power MOSFET with a flexible negative voltage (such as –3.5 V) to accelerate the turn-off speed. The experimental results demonstrate the significant efficiency improvement over the conventional VSD with a 5.62 W loss reduction at 1.2 V/30 A output and a 3.84 W loss reduction at 1.3 V/30 A with 12 V input in 1 MHz switching frequency. The comparison between the proposed CSD and the existing CSD in [23] and [24] demonstrates that the CSD proposed in this paper is a better alternative for next-generation VRs. More importantly, the basic idea presented in this paper can also be extended to other existing CSD drivers to further improve their performance with a high output current.

References

[1] *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD), Std. 11.1 Design Guidelines*, Sep. 2009

[2] Y. Dong, J. Zhou, F. C. Lee, M. Xu, and S. Wang, "Twisted core coupled inductors for microprocessor voltage regulators," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2536–2545, Sep. 2008.

[3] D. D.-C. Lu, J. C. P. Liu, F. N. K. Poon, and B. M. H. Pong, "A single phase voltage regulator module (VRM) with stepping inductance for fast transient response," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 417–424, Mar. 2007.

[4] Y. Han, O. Leitermann, D. A. Jackson, J. M. Rivas, and D. J. Perreault, "Resistance compression networks for radio-frequency power conversion," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 41–53, Mar. 2007.

[5] T. Hashimoto, M. Shiraishi, N. Akiyama, T. Kawashima, T. Uno, and N. Matsuura, "System in package (SiP) with reduced parasitic inductance for future voltage regulator," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1547–1533, Jun. 2009.

[6] L. Huber, K. Hsu, M. M. Jovanovic, D. J. Solley, G. Gurov, and R. M. Porter, "1.8-MHz, 48-V resonant VRM: Analysis, design, and performance evaluation," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 79–88, Jan. 2006.

[7] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Dordrecht, The Netherlands: Kluwer, 2001.

[8] Y. Xiong, S. Sun, H. Jia, P. Shea, and Z. J. Shen, "New physical insights on power MOSFET switching losses," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 525–531, Feb. 2009.

[9] T. Lopez, G. Sauerlaender, T. Duerbaum, and T. Tolle, "A detailed analysis of a resonant gate driver for PWM applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo. Asia Pacific Econ. Cooperation (APEC)*, 2003, pp. 873–878.

[10] D. A. Grant and J. Gowar, *Power MOSFET Theory and Applications*. New York: Wiley, 1989.

[11] Y. Ren, M. Xu, J. Zhou, and F. C. Lee, "Analytical loss model of power MOSFET," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 310–319, Mar. 2006.

[12] Y. Xiao, H. Shah, R. Natarajan, and E. J. Gutmann, "Analytical modeling and experimental evaluation of interconnect parasitic inductance on MOSFET switching characteristics," in *Proc. IEEE Appl. Power Electron. Conf. Expo. Asia Pacific Econ. Cooperation (APEC)*, 2004, vol. 1, pp. 516–521.

[13] G. Spiazzi, P. Mattavelli, and L. Rossetto, "Effects of parasitic components in high-frequency resonant drivers for synchronous rectification MOSFETs," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 2082–2092, Jul. 2008.

[14] D. Maksimovic, "A MOS gate drive with resonant transitions," in *Proc. IEEE Power Electron. Spec. Conf. Postsecondary Electron. Standard Council (PESC)*, 1991, pp. 527–532.

[15] Y. Chen, F. C. Lee, L. Amoros, and H. Wu, "A resonant MOSFET gate driver with efficient energy recovery," *IEEE Trans. Power Electron.*, vol. 19, no. 2, pp. 470–477, Mar. 2004.

[16] T. Ren-Huei and C. Chern-Lin, "A low-consumption regulated gate driver for power MOSFET," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 532–539, Jan. 2009.

[17] K. Yao and F. C. Lee, "A novel resonant gate driver for high frequency synchronous buck converters," *IEEE Trans. Power Electron.*, vol. 17, no. 2, pp. 180–186, Mar. 2002.

[18] Y. Ren, M. Xu, Y. Meng, and F. C. Lee, "12 V VR efficiency improvement based on two-stage approach and a novel gate driver," in *Proc. IEEE Power Electron. Spec. Conf. Postsecondary Electron. Standard Council (PESC)*, 2005, pp. 2635–2641.

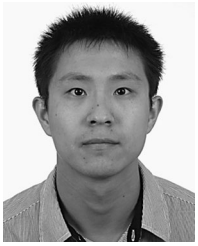
[19] Z. Zhang, W. Eberle, Z. Yang, Y. F. Liu, and P. C. Sen, "Optimal design of resonant gate driver for buck converter based on a new analytical loss model," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 653–666, Mar. 2008.

[20] Z. Yang, S. Ye, and Y. F. Liu, "A new resonant gate drive circuit for synchronous buck converter," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1311–1320, Jul. 2007.

[21] Z. Yang, S. Ye, and Y. F. Liu, "A new dual channel resonant gate drive circuit for low gate drive loss and low switching loss," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1574–1583, May 2008.

[22] Z. Zhang, W. Eberle, P. Lin, Y. F. Liu, and P. C. Sen, "A 1-MHz high-efficiency 12-V buck voltage regulator with a new current-source gate driver," *IEEE Trans Power Electron.*, vol. 23, no. 6, pp. 2817–2827, Nov. 2008.

[23] W. Eberle, Z. Zhang, Y. F. Liu, and P. C. Sen, "A high efficiency synchronous buck VRM with current source gate driver," in *Proc. IEEE Power Electron. Spec. Conf. Postsecondary Electron. Standard Council (PESC)*, 2007, pp. 21–27.
[24] W. Eberle, Z. Zhang, Y. F. Liu, and P. C. Sen, "A current source gate driver achieving switching loss savings and gate energy recovery at 1-MHz," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 678–691, Mar. 2008.
[25] Z. Zhang, J. Fu, Y. F. Liu, and P. C. Sen, "A new discontinuous current source driver for high frequency power MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2009, pp. 1655–1662.
[26] Z. Zhang, J. Fu, Y. F. Liu, and P. C. Sen, "Discontinuous current source drivers for high frequency power MOSFETs," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1863–1876, Jul. 2010.
[27] W. Eberle, Z. Zhang, Y. F. Liu, and P. C. Sen, "A practical switching loss model for buck voltage regulators," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 700–713, Mar. 2009.
[28] SIMetrix Technologies. SIMetrix. (2010). [Online]. Available: http://www. simetrix. co.uk/.
[29] Vishay Intertechnology, Inc. Datasheet of SI7386DP, (Mar. 2008). [Online]. Available: http://www. vishay.com/docs/73108/73108.pdfy.
[30] J. Wang, "On-chip inductors and transformers," in *Proc. IEEE Appl. Power Electron. Conf. Expo. Asia Power Electron. Council (APEC)*, 2010, pp. 3–19.
[31] J. Sun, M. Xu, Y. Ren, and F. C. Lee, "Light-load efficiency improvement for buck voltage regulators," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 742–751, Mar. 2009.
[32] P. Zumel, C. Fernández, A. de Castro, and O. Garcia, "Efficiency improvements in multiphase converter by changing dynamically the number of phases," in *Proc. IEEE Power Electron. Spec. Conf. Postsecondary Electron. Standard Council (PESC)*, 2006, pp. 1–6.
[33] L. T. Jakobsen, O. Garcia, J. A. Oliver, P. Alou, J. A. Cobos, and M. A. E. Andersen, "Interleaved buck converter with variable number of active phases and a predictive current sharing scheme," in *Proc. IEEE Power Electron. Spec. Conf. Postsecondary Electron. Standard Council (PESC)*, 2008, pp. 3360–3365.



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Lusheng Ge, photograph and biography not available at the time of publication.